

Write a short code segment, using the LOOP instruction, that calls the “CallMe” subroutine 25 times.

What is the difference between the IRET and RET (far) instructions?

What happens during a read bus cycle of 8086 microprocessor in each of the following states ?

- a) T1 : ALE , will activated at T1 only  
DT/R , will activated at T1 – T4  
IO/M , will activated at T1 – T4  
  
BHE , will activated at T1- T4
- b) T2 : DEN , will activated at T2 – T4  
RD , will activated at T2- T4
- c) T3 : wait state will be inserted if it needed , and used to all memory to access data
- d) T4 : all control signal addresses will be deactivated in preparation for the next clock cycle

-What are the operational modes of an Intel 8086 microprocessor and how do they differ?

-Which mode of 8086 is required for the multiprocessor system?

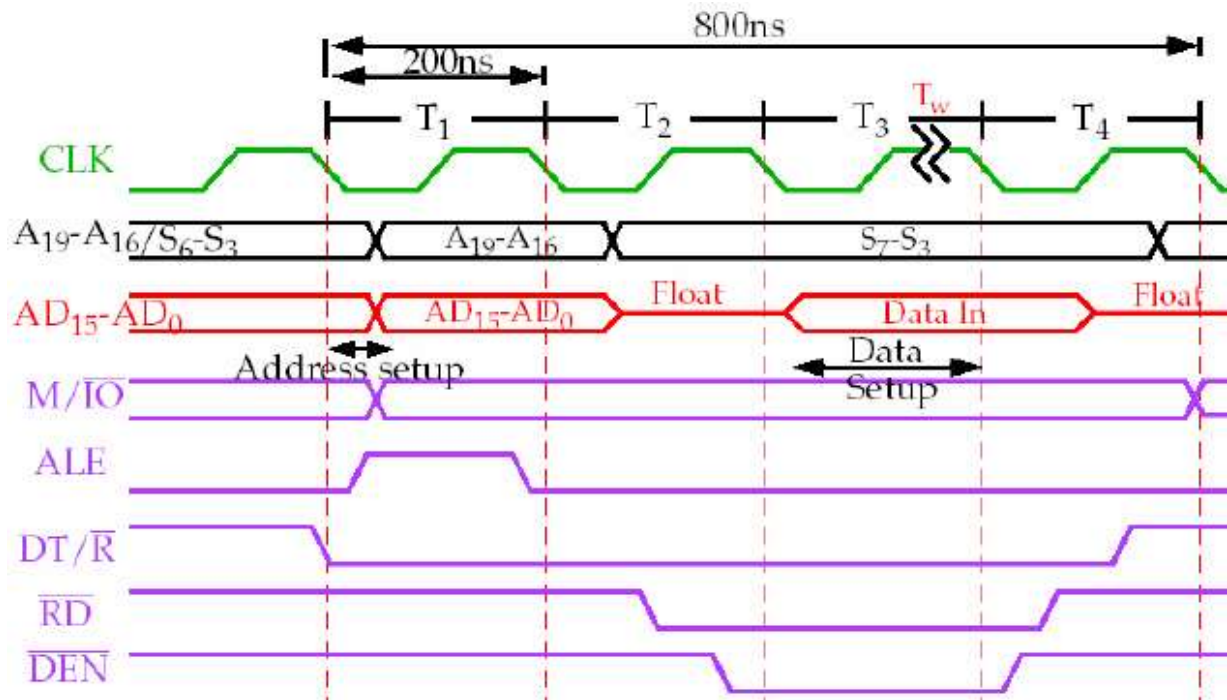
-What main function is provided by 8288 bus controller when used with 8086/8088 maximum mode operation?

- a : MOV AH,DS:BYTE PTR[F3C6]      b : MOV CX,DS:WORD PTR[0ABE]
- c : MOV IP,DS: [0001]              d : MOV AX,SS:[000BH]

find out the information required to complete table below from the above instructions

ADDRESS	DATA TYPE	BHE (ACTIVE LOW)	A0	BUS CYCLES	DATA LINES USED

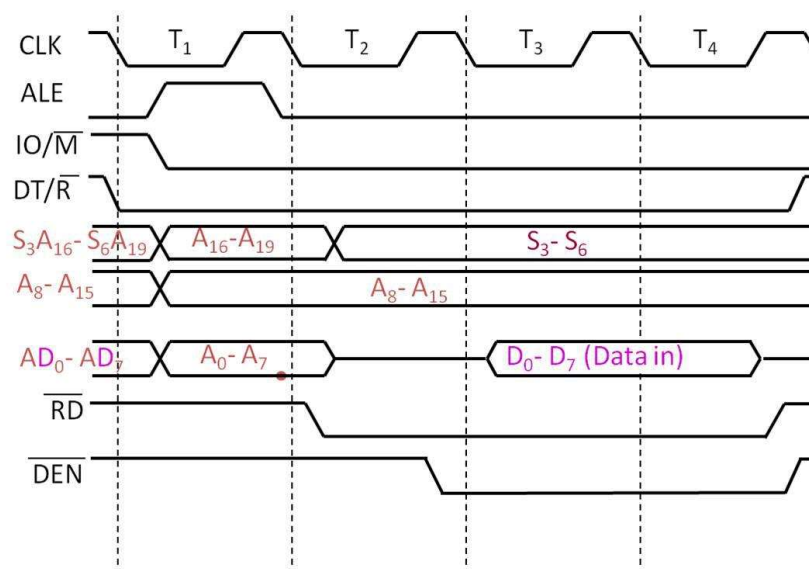
-For 8088 system , draw the timing diagram for the following instruction : Mov AL, [1000] ?  
 ASSUME DS=1000H



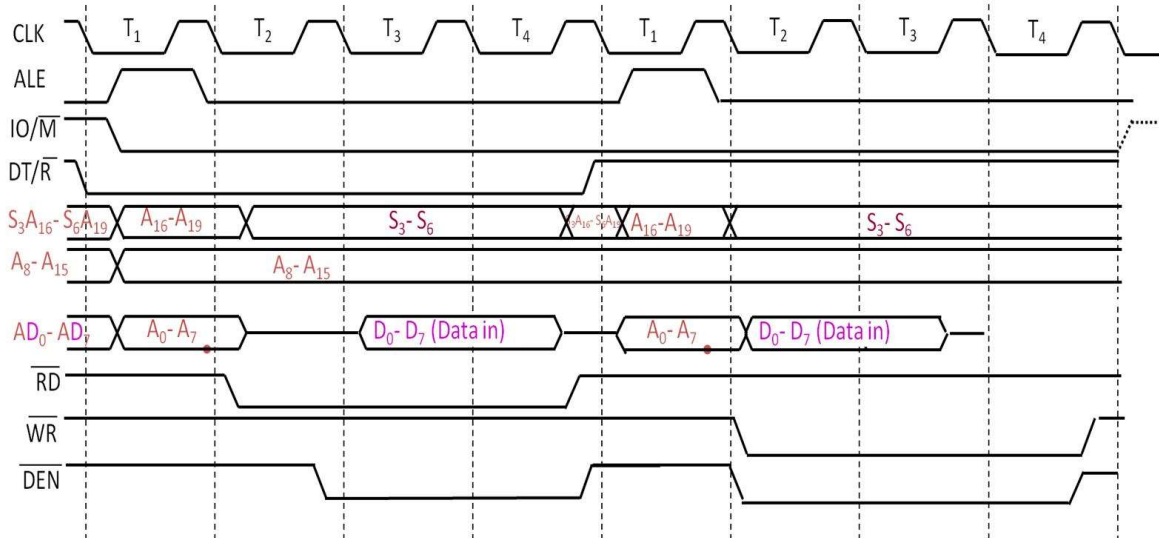
Assume that; DI=1645h , SI= 4759h , DS= 8000h , data in DS:DI = 1066h , data in DS:SI = 5522h

Draw a system bus timing diagram required to execute the following instructions by the microprocessor 8088;

1- **MOV BL, [DI]**



## 2- INC byte ptr [SI]



Why a separate write control signal is needed for each bank?

ONCE THE MICROPROCESSOR WRITE A DATA WORD TO THE MEMORY , IT NEEDS TO ACTIVATE THE CORRECT OR THE TARGET BANK, BASED ON THE ADDRESS EVEN OR ODD.